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(54) Improvements in or relating to manufacture of semiconductor devices of high breakdown voltage

(57) A method is provided for the manufacture of high voltage semiconductor devices with at least one planar junction with a variable charge concentration. The method consists in doping with impurities of a same type, in a region 1 of monocrystalline semiconductor material, a first zone 3, and then a second zone 4 which includes the first, and so on, and in carrying out a subsequent heat treatment so as to provide a planar junction 8 with a stepped profile and a concentration of impurities which decreases from the centre to the periphery in a predetermined range. In this way the intensity of the surface electric field, when the junction is reverse biased, is reduced as a result of which it is possible to provide planar junctions having very high breakdown voltages of some thousands of volts.

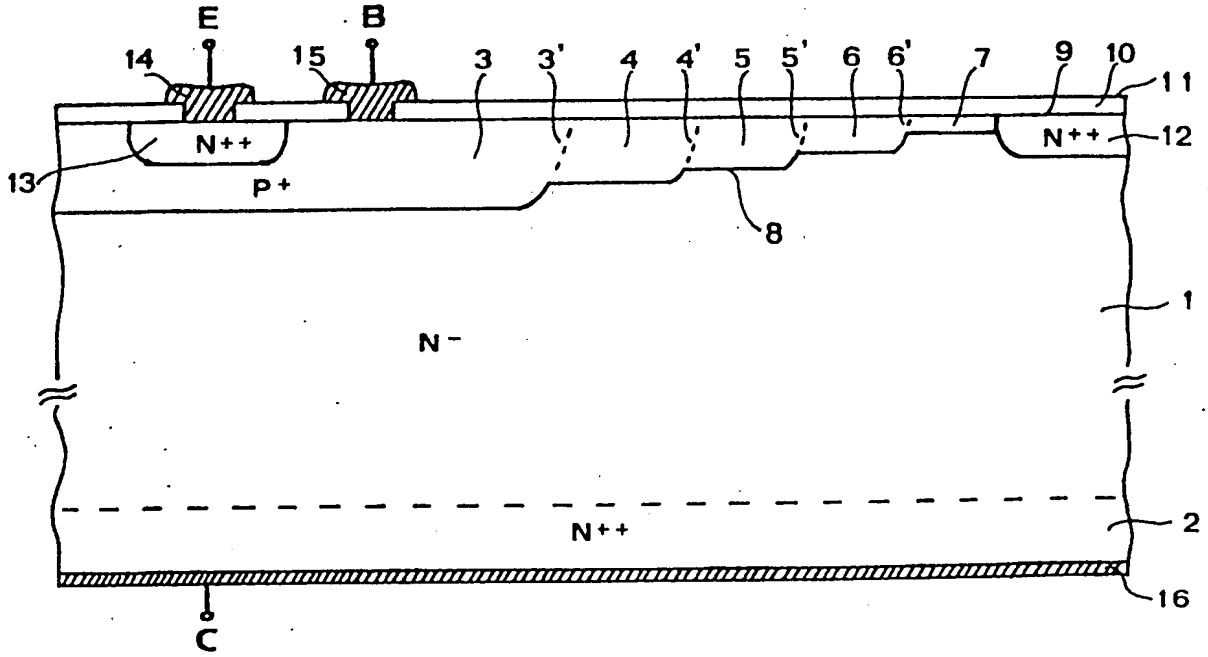

FIG 1

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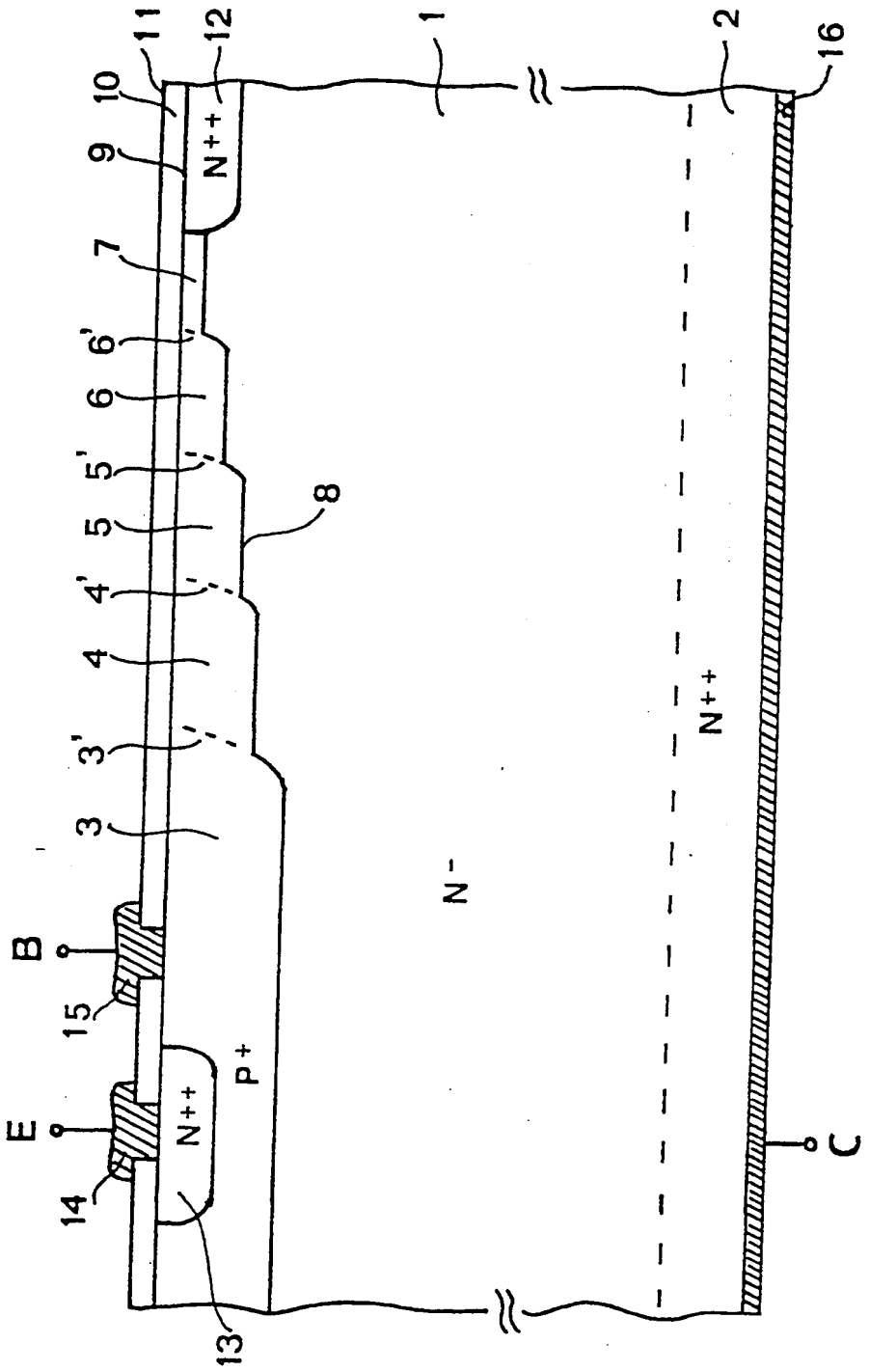

FIG 1

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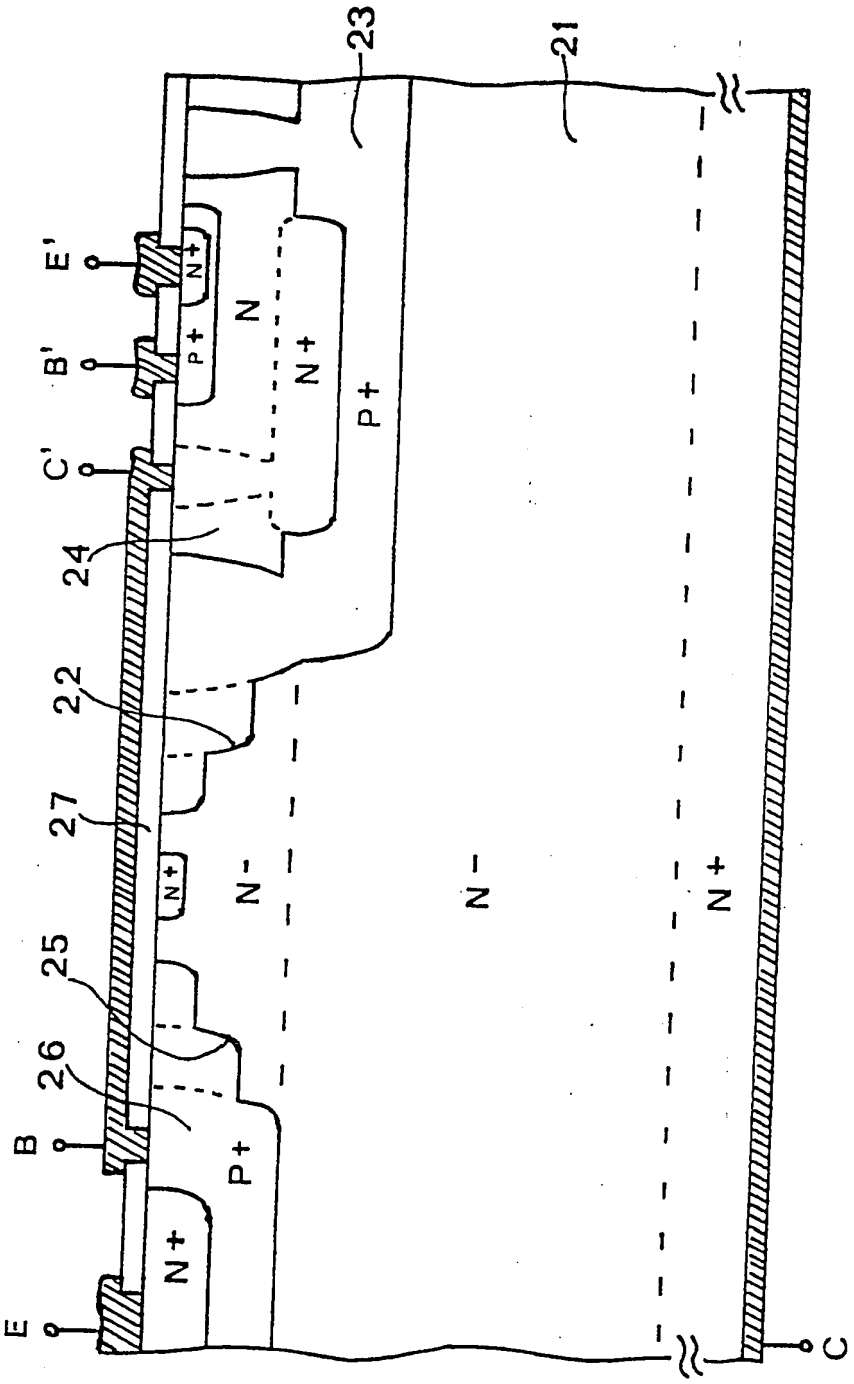

FIG 2

SPECIFICATION

Improvements in or relating to manufacture of semiconductor devic s of high br akdown voltage

The invention relates to electronic semiconductor devices and more precisely to devices comprising at least one planar P-N junctions, such as diodes, bipolar transistors and integrated circuits, designed to operate at high voltages, for instance at voltages of some thousands of volts.

It is known that, in order to achieve and maintain high voltages in semiconductor devices with planar P-N junctions, current technology provides various possibilities. All these have the common objective of providing a junction which comes as close as possible to the ideal case of a junction with plane, parallel surfaces having an infinite extension.

A known device, disclosed in the publication "Solid State Electronics", 1972, Vol 15, pp 93–105, involves the use of a metallic field plate which extends over a layer of silicon oxide of constant thickness above the edge of a planar junction. The effect of this structure, when the junction is reverse biased, is to widen the space charge region below the field plate and to increase the radius of curvature of the equipotential lines, thereby causing a reduction of the electrical field and consequently an increase of the breakdown voltage. However, in this case the breakdown voltage is restricted to 600 V as a result of the edge effects which the field plate introduces into the junction.

The above publication also describes a planar junction structure with the metallic field plate disposed on a layer of silicon oxide of variable thickness which enables the above-mentioned voltage limit to be exceeded by modifying the boundary conditions and thereby increasing the breakdown voltage to a value of approximately 1000 V.

A further known possibility is to modify the terminal portion of the junction. This technique, known by some as "Junction Termination Extension" (JTE) or by others as "Implanted Field Plate" is described, for example, in the publication "IEEE Transaction on Electron Devices", 1983, Vol ED-30, pp 954–957. Figs. 10 and 11 in particular of this publication show a P–N junction terminating with two implanted zones. This structure makes it possible to reach a breakdown voltage of 1400 V, using an N doped substrate with $1.15 \cdot 10^{14}$ atoms/cm^3 in which an impurity of p-type is diffused at a concentration of 10^{17} atoms/cm^3 and in which two JTE zones with surface concentrations of $3 \cdot 10^{15}$ and $1 \cdot 10^{15}$ atoms/cm^3 are respectively implanted.

Nowadays, stable, reliable and economically viable electronic semiconductor devices with P-N junctions capable of withstanding voltages of some thousands of volts are required. These devices are required, for example, in the fields of high voltage supply devices, radar, electromedical apparatus using X-rays and, in general, in any field requiring the use of high voltages.

According to the invention, there is provided a method as defined in the appended claim 1 or 14. Preferred embodiments are defined in the other appended claims.

A preferred method consists in treating a substrate of monocrystalline semiconductor material having a low concentration of impurities and a predetermined electrical conductivity with the following operations: doping with an impurity of opposite conductivity to that of the substrate of a first zone of the substrate with a first predetermined quantity of impurity, after which this first zone and a second zone which comprises the first zone are doped with a second predetermined quantity of impurity, and then, if necessary, the first, second and a third zone which comprises the first and second zones are doped with a third predetermined quantity of impurity, and so on until the required number of doping operations have been carried out on zones of increasing area, but with a decreasing concentration of impurities.

These doping operations are followed by a heat treatment which causes the diffusion of the impurities in the substrate up to the required depth and enables the achievement of a P-N junction whose stepped profile has a concentration of impurities which decreases from the centre of the periphery for a predetermined extension, as the concentrations of doping agent are added together zone by zone.

The invention will be further described, by way of example, with reference to the accompanying drawings, in which:

Figure 1 shows a section, not to scale, of a portion of a silicon chip comprising an n-p-n power transistor having a very high voltage collector-base junction, and

Figure 2 shows a section, not to scale, of a portion of a silicon chip comprising a monolithic device formed by a bipolar power transistor and by a integrated circuit, both integrated on the same chip.

The device with the very high voltage P-N junction is described with reference to Fig. 1, this device being constructed by means of the following method steps, which are described with reference, for simplicity of explanation, to a chip of a monocrystalline silicon wafer.

Stage 1: Use is made of a substrate 1 of monocrystalline silicon of n-type and a low

concentration of doping agent, or with a resistivity value of more than 500 ohm/cm and a thickness of 425 μm. The surfaces of the substrate are than oxidised.

Stage 2: A face of the substrate of the chip, called the "front" of the chip in the following description, is subjected t an operation, by means of photomasking and etching, to remove the layer of oxide 10 in the area of the surface above the region 3. This surface with the oxide removed and with a width of 3000 μm is then subjected to ion implantation of a p-type doping agent or of a conductivity opposite to the type of conductivity in region 1. This doping agent is constituted by boron which is implanted at a dosage of 5×10^{14} atoms/cm² with an implantation energy of 100 KeV.

Alternatively, given the high doping level of this region, the boron may be deposited by means of a boron nitride BN (A) source of a-type at 950°C rather than implanted.

Stage 3: The layer 10 of oxide is removed from the surface above the region 4 on the front of the chip by photomasking and etching. Since the surface above region 3 has already had its oxide removed, the entire surface of the continuous zone 3–4, the zone 4 having a width of 180 μm, is free from oxide. The entire surface of this zone 3–4 is then subjected to ion implantation of the same p-type doping agent used for doping the region 3, ie boron at a dosage of 1.5×10^{12} atoms/cm² at an implantation energy of 180 KeV.

Stage 4: The steps described above are repeated so as to free the entire surface of the continuous zone 3, 4, 5 (the zone 5 having a width of 180 μm) from oxide and implant the same p-type doping agent already used, ie boron, at a dosage of 1.5×10^{12} atoms/cm² at an implantation energy of 180 KeV.

Stage 5: The steps described above are repeated so as to free the entire surface of the continuous zone 3, 4, 5, 6 (the zone 6 having a width of 180 μm) from oxide and implant the same p-type doping agent already used, ie boron, at a dosage of 2.5—10^{12} atoms/cm² at an implantation energy of 180 KeV.

Stage 6: The steps described above are finally repeated so as to free the entire surface of the continuous zone 3, 4, 5, 6, 7 (the zone 7 having a width of 90 μm) from oxide and implant the same p-type doping agent already used, ie boron, at a dosage of 0.2×10^{12} atoms/cm² at an implantation energy of 180 KeV.

In conclusion the dosages of boron implanted remain confined in the zones 3, 4, 5, 6, 7 which together provide the base region of the transistor, and the successive implantations are added in each zone, as shown in the following table:

ZONE	WIDTH (μm)	IMPLANTATION DOSAGE (atoms/cm²)	CUMULATIVE IMPLANTATION DOSAGE (atoms/cm²)
3	3000	5.0×10^{14}	505.7×10^{12}
4	180	1.5×10^{12}	5.7×10^{12}
5	180	1.5×10^{12}	4.2×10^{12}
6	180	2.5×10^{12}	2.7×10^{12}
7	90	0.2×10^{12}	0.2×10^{12}

Stage 7: After the completion of the above-mentioned implantation operations, the p-type doping agent, boron, is diffused at 1200°C for 8 hours so as to obtain a single base region having, for the purposes of the production method, the profile 8 shown in Fig. 1. It should be noted that the depth of this profile 8 within the region 1 below the surface 9 of the oxide layer 10 is of substantially no relevance for the purposes of the invention, whereas the distribution of the quantity of the doping agent within the base region 3, 4, 5, 6, 7 of the transistor is of importance. This has to be understood as the subsequent high temperature operations tend to make the profile 8 of the base region deeper within the collector region 1 of the chip.

Stage 8: (The subsequent stages are of relatively little relevance to the invention, but will be described for the sake of completeness).

The region of low resistivity is then formed by diffusing into the entire surface from the "rear" of the chip, by means of the removal of its covering oxid , the same n-type doping agent, for example phosphorus, already present in the whole of the silicon substrate 1. The collector region of the transistor is thus provided with the required electrical characteristics.

Stage 9: This is followed by the simultaneous formation of the emitter region 13 of the

transistor and the region 12 called "channel stopper", whose function is known to persons skilled in the art, by means of the diffusion of an n-type doping agent, for example phosphorus, from the front of the chip into the regions 3 and 1 respectively up to the required depth.

Stage 10: The final step involves the formation of the metallizations 14, 15 and 16, shown in dashed lines in Fig. 1, required for the contacts of the electrodes of the emitter E, the base B and the collector C, respectively, of the transistor.

Although a single embodiment of the present invention has been described and illustrated, it is obvious that many modifications and variations may be made thereto, without departing from the scope of the invention. For example, with reference to Fig. 1, the p-type base region 3, 4, 5, 6, 7 which, together with the n-type collector region 1 of opposite conductivity forms the very high voltage P–N junction, may be formed by a variable number of cumulatively implanted zones with a minimum of at least one (in this latter case the junction 8 shown in Fig. 1 is modified such that it terminates along the section of curve 4' under the surface 9 covered by the oxide 10).

This number of cumulatively implanted zones >1 in the base region of the transistor depends which particular on the maximum voltage with the P-N junction must withstand without breaking down. The higher the number of cumulatively implanted zones, the higher the voltage which the junction may withstand. For example, the junction shown in Fig. 1 with four cumulatively implanted zones withstands more than 3700 V.

Also, the method described for the manufacture of an n-p-n transistor may be applied, with the necessary modifications known to persons skilled in the art, to the manufacture of a p-n-p transistor, in which the junction having a very high breakdown voltage is obtained from a p-type substrate in which n-type impurities are implanted and diffused.

The horizontal geometry of the P-N junction may be of any shape for instance as in the case of interdigitated structures forming the base and emitter regions of a transistor.

The invention does not only apply to single or discrete devices such as diodes, bipolar transistors, MOS transistors, but to all semiconductor devices where it is necessary to provide at least one very high voltage P-N junction. For example, Fig. 2 shows a section, not to scale, of a portion of a silicon chip comprising a monolithic device formed by a bipolar power transistor, shown on the left-hand side of the Figure and by an integrated circuit, of which a single transistor is shown in the right-hand part of the Figure, these being connected together electrically by metallized tracks lying on the oxide layer 27. Two high voltage P-N junctions are shown; the first junction 25 forming the collector-base junction of the power transistor and the second junction 22 forming the junction of the isolation region 23 which surrounds the integrated circuit.

The high voltage junction 22 in the structure of the device shown in Fig. 2 is designed to cause the isolation region 23 to withstand the same voltage supplied to the high voltage collector-base junction 25 of the power transistor. It should be noted that this junction 22 is only present from the high voltage portion of the region 21, forming the collector region of the power transistor of the monolithic device, and not from the low voltage portion of the region 24 forming the collector region of the transistor of the integrated circuit. After having diffused and thus obtained the horizontal isolation layer 23, and after forming the buried layers in the integrated circuit and causing an epitaxial growth of n-doped monocrystalline silicon over the entire surface of the substrate 21, ion implantation is carried out followed by the diffusion of the p-type doping agents so as to form simultaneously both the high voltage P-N junctions 22 and 25 in accordance with the method steps described above. However, in contrast to the transistor of Fig. 1, in which the junction 8 is formed by four cumulative zones, in the device of Fig. 2 both the junctions 22 and 25 have two cumulative zones above to withstand a voltage of at least 1000 V

The invention may also be applied to bipolar and unipolar devices of lateral type in which the flow of the charge carriers takes place in a horizontal direction. For example, a high voltage lateral MOS transistor may be formed with its drain region having a concentration of impurities which decreases from the centre to the periphery in a stepped profile.

CLAIMS

1. A method of making a semiconductor device comprising a substrate of monocrystalline semiconductor material having a surface partially covered by a layer of insulating material, a first region of a first type of conductivity formed in the substrate and at least partially confining, with the said surface, a second region of a second type of conductivity opposite to the first and embedded in the first region so as to form with the first region a planar junction, in which the second region is formed by successive operations of doping with impurities of the same type in predetermined quantities of zones of the first region comprising when necessary the zones doped by means of the previous operation and with a high temperature treatment for the simultaneous diffusion of the impurities in the substrate so that the concentration of impurities in the second region decreases from the centre of the periphery with a stepped profile.

2. A method as claimed in claim 1, in which the number of successive doping operations,

the quantity of impurities and the horizontal extension of each zone of the second region, forming the planar junction with the first region, are optimised so as to reduce to a minimum the mean intensities of the surface electrical field for a predetermined breakdown voltage of the junction.

3. A method as claimed in claim 1 or 2, in which the first region of the two adjacent regions having conductivity of opposite type and forming the planar junction is formed with a lower concentration of impurities than the minimum concentration of the second region.

4. A method as claimed in any one of the preceding claims, in which the successive doping operations for the formation of the second region are carried out by ion implantation.

5. A method as claimed in claim 4, in which the first region of the device is formed by monocrystalline silicon and the impurities implanted for the formation of the second zone comprise atoms of boron, each implanted zone of the second region having a width of at least 10 μm.

6. A method as claimed in claim 5, in which the second zone is formed with three adjacent implanted zones, and the first central zone receives a cumulative implantation dosage of between 1 E 14 and 1 E 15, the second, or intermediate, zone, a dosage of between 2 E 12 and 2 E 13 and the third peripheral zone a dosage of between 1 E 12 and 1 E 13 atoms/cm^2.

7. A method as claimed in claim 5, in which the second region is formed by four adjacent implanted zones, and the first central zone receives a cumulative implantation dosage of between 1 E 14 and 1 E 15, the second zone a dosage of between 3 E 12 and 3 E 13, the third zone a dosage of between 2 E 12 and 2 E 13 and the fourth, peripheral zone a dosage of between 1 E 12 and 1 E 13 atoms/cm^2.

8. A method as claimed in claim 5, in which the second region is formed by five adjacent implanted zones, and the first central zone receives a cumulative implantation dosage of between 1 E 14 and 1 E 15, the second zone a dosage of between 4 E 12 and 4 E 13, the third zone a dosage of between 3 E 12 and 3 E 13, the fourth zone a dosage of between 2 E 12 and 2 E 13 and the fifth peripheral zone a dosage of between 1 E 12 and 1 E 13 atoms/cm^2.

9. A method as claimed in claim 5, in which the second region is formed by six adjacent implanted zones, and the first central zone receives a cumulative implantation dosage of between 1 E 14 and 1 E 15, the second zone a dosage of between 5 E 12 and 5 E 13, the third zone a dosage of between 4 E 12 and 4 E 13, the fourth zone a dosage of between 3 E 12 and 3 E 13, the fifth zone a dosage of between 2 E 12 and 2 E 13 and the sixth peripheral zone a dosage of between 1 E 12 and 1 E 13 atoms/cm^2.

10. A method as claimed in claim 5, in which the second region is formed by seven adjacent implanted zones, and the first central zone receives a cumulative implantation dosage of between 1 E 14 and 1 E 15, the second zone a dosage of between 6 E 12 and 6 E 13, the third zone a dosage of between 5 E 12 and 5 E 13, the fourth zone a dosage of between 4 E 12 and 4 E 13, the fifth zone a dosage of between 3 E 12 and 3 E 13, the sixth zone a dosage of between 2 E 12 and 2 E 13 and the seventh peripheral zone a dosage of between 1 E 12 and 1 E 13 atoms/cm^2.

11. A method as claimed in claim 5, in which the second region is formed by eight adjacent implanted zones, and the first central zone receives a cumulative implantation dosage of between 1 E 14 and 1 E 15, the second zone a dosage of between 7 E 12 and 7 E 13, the third zone a dosage of between 6 E 12 and 6 E 13, the fourth zone a dosage of between 5 E 12 and 5 E 13, the fifth zone a dosage of between 4 E 12 and 4 E 13, the sixth zone a dosage of between 3 E 12 and 3 E 13, the seventh zone a dosage of between 2 E 12 and 2 E 13 and the eight peripheral zone a dosage of between 1 E 12 and 1 E 13 atoms/cm^2.

12. A method as claimed in claim 5 in which the second region is formed by nine adjacent implanted zones, and the first central zone receives a cumulative implantation dosage of between 1 E 14 and 1 E 15, the second zone a dosage of between 8 E 12 and 8 E 13, the third zone a dosage of between 7 E 12 and 7 E 13, the fourth zone a dosage of between 6 E 12 and 6 E 13, the fifth zone a dosage of between 5 E 12 and 5 E 13, the sxth zone a dosage of between 4 E 12 and 4 E 13, the seventh zone a dosage of between 3 E 12 and 3 E 13, the eight zone a dosage of between 2 E 12 and 2 E 13 and the ninth peripheral zone a dosage of between 1 E 12 and 1 E 13 atoms/cm^2.

13. A method of making a semiconductor device substantially as hereinbefore described with reference to and illustrated in the accompanying drawings.

14. A method of making a semiconductor device, comprising doping a first surface region of a semiconductor substrate of a first conductivity typ with an impurity of a second conductivity type, doping a second surface region which contains the first surface region with the impurity of the second conductivity type, and diffusing the impurity of the second conductivity type in the substrate.

15. A semiconductor device made by a method as claimed in any one of the preceding claims.

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